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1 [C2MP: a cache-coherent, distributed memory multiprocessor-system](#)

D. E. Marquardt, H. S. Alkhatib

August 1989 **Proceedings of the 1989 ACM/IEEE conference on Supercomputing**Full text available: [pdf\(1.22 MB\)](#)
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Current research into the problems of cache coherency in multiprocessor (MP) systems, has primarily focused on bus based memory interconnection networks (M-ICN) and the use of various types of "snooping" cache coherency protocols. Bus bandwidth limitations can be alleviated through the use of wider bandwidth general interconnection structures, such as a crossbar switch. However, if private caches are used, the cache coherency problem becomes mul ...

2 [Generating highly-routable sparse crossbars for PLDs](#)

Guy Lemieux, Paul Leventis, David Lewis

February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**Full text available: [pdf\(952.31 KB\)](#)
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A method for evaluating and constructing sparse crossbars which are both area efficient and highly routable is presented. The evaluation method uses a network flow algorithm to accurately compute the percentage of random test vectors that can be routed. The construction method attempts to maximize the spread of the switch locations, such that any given subset of input wires can connect to as many output wires as possible. Based on Hall's Theorem, we argue that this increases the likelihood ...

3 [Classification Categories and Historical Development of Circuit Switching Topologies](#)

George Broomell, J. Robert Heath

June 1983 **ACM Computing Surveys (CSUR)**, Volume 15 Issue 2Full text available: [pdf\(2.55 MB\)](#)
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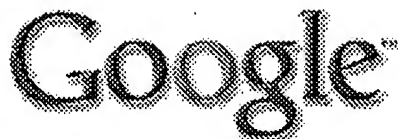
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